WHAT IS CLAIMED IS

1. A test pattern generator for generating, at least once, a pattern sequence cluster composed of a plurality of pattern sequences with a given number of bits and a given number of times, the circuit comprising:

an identical pattern sequence generator which generates pattern sequences in the pattern sequence cluster which are all identical; and

a bit-flipping sequence generator which uses the pattern sequence cluster generated by the identical pattern sequence generator as input and flips some bits in pattern sequences in the pattern sequence cluster and changes the positions of bits to be flipped in patterns according to the pattern sequence cluster, and pattern sequence number and time in pattern sequence within the pattern sequence cluster.

2. The test pattern generator according to Claim 1, the identical pattern sequence generator having a linear feedback shift register and at least one register which holds the register initial value (seed) in the linear feedback shift register while one of the pattern sequence clusters is being generated..

3. The test pattern generator according to Claim 1, the bit-flipping sequence generator including a controller which controls bit-flipping so that an input pattern sequence cluster comprises, in whole or in part, such pattern sequences as ones without flipped bits,

ones with all or some flipped bits in one pattern and ones with all or some flipped bits in plural consecutive patterns or patterns at regular intervals, the interval being equivalent to a given number of patterns.

4. A test pattern generator including:

a plurality of linear feedback shift registers; and

a circuit for controlling a mode in which the plural linear feedback shift registers each generate pseudo-random patterns, and a mode in which all or some of the linear feedback shift registers work together as one shift register to generate patterns.

5. A semiconductor integrated circuit, wherein the test pattern generator as defined in Claim 1 or the bit-flipping sequence generator is integrated with a circuit to be tested, and input signal lines on the scan chain provided in the circuit to be tested or external input signal lines to the circuit to be tested are connected with output signal lines of the test pattern generator or the bit-flipping sequence generator.

6. A semiconductor integrated circuit test method in which test pattern signals are applied to the circuit to be tested which has scan chain input signal lines or external input signal lines and the pattern of response from the circuit under test is compared with the expected pattern, the process of generating the

above test pattern signals comprising the steps of:

generating identical pattern sequences in a cluster of plural pattern sequences with a given number of bits and a given number of times, all of which are identical; and

flipping some bits in pattern sequences in the pattern sequence cluster composed of identical pattern sequences and changing the positions of bits to be flipped according to the pattern sequence cluster, and pattern sequence number and time in pattern sequence in the pattern sequence cluster.

7. The test method according to Claim 6, the process of generating identical pattern sequences comprising:

a first step of generating a test pattern set for detection of assumed faults;

a second step of, taking the test pattern set as pattern sequence groups, classifying the pattern sequence groups into clusters in each of which the pattern sequences are identical in the set of combinations of time in pattern sequence and bit position in pattern to be set, and their Hamming distances are all under a predetermined distance; and

a third step of generating, for each of the pattern sequence clusters, pattern sequences as decided by majority with regard to time in pattern sequence and bit position in pattern from the pattern sequences belonging to it,.

8. The test method according to Claim 6, the process of generating identical pattern sequences comprising:

a first step of generating a test pattern set for detection of presumed faults;

a second step of, taking the test pattern set as pattern sequence groups, classifying the pattern sequence set into clusters in each of which the pattern sequences are identical in the set of combinations of time in pattern sequence and bit position in pattern to be set and their Hamming distances are all under a predetermined distance;

a third step of generating, for each of the pattern sequence clusters, pattern sequences as decided by majority with regard to time in pattern sequence and bit position in pattern from the pattern sequences belonging to it;

a fourth step of encoding the pattern sequences decided at the preceding step into LFSR register initial values (seeds); and

a fifth step of selecting, from the LFSR register seeds obtained at the preceding step, ones which can be used to newly detect faults when developed for a pattern sequence cluster, or ones which include test patterns.

9. A method for generating at least once a pattern sequence cluster composed of a plurality of pattern sequences with a given number of bits and a

given number of times, wherein, in the pattern sequence cluster, a reference pattern sequence is generated as a reference, and, the cluster comprises, in whole or in part, with respect to the reference pattern sequence, such pattern sequences as ones without flipped bits, ones with all or some flipped bits in one pattern and ones with all or some flipped bits in consecutive patterns or patterns at regular intervals, the interval being equivalent to a given number of patterns.

10. A semiconductor integrated circuit test method, wherein a pattern sequence cluster composed of a plurality of pattern sequences having the number of bits and the maximum length of scan chain which depend on the number of scan chains and the number of external input terminals, and also having the number of times which depends on the unit test sequence length is generated according to the pattern generating process as disclosed in Claim 9 and the pattern sequence cluster is applied to a circuit under test at least once.

11. The semiconductor integrated circuit test method according to Claim 10, the process of generating the reference pattern sequence comprising:

a first step of generating a test pattern set for detection of assumed faults;

a second step of, taking the test pattern set as pattern sequence groups, classifying the pattern sequence set into clusters in each of which the pattern

sequences are identical in the set of combinations of time in pattern sequence and bit position in pattern to be set and their Hamming distances are all under a predetermined distance; and

a third step of generating, for each of the pattern sequence clusters, a pattern sequence as decided by majority with regard to time in pattern sequence and bit position in pattern from the pattern sequences belonging to it, and defining it as the reference pattern sequence.

12. A semiconductor integrated circuit test method, in which, in the process of generating test patterns by scan chain shift for a full scan design semiconductor integrated circuit, a step of scan chain shift without any change in all scan chain inputs is provided to set an identical logical value on neighboring storage elements on a scan chain, and the resulting pattern is used as a test pattern.